공면 배선구조의 시그널 인테그러티 검증

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Signal Integrity Verification in Coplanar Interconnect Line
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요 약
본 연구에서는 집적회로의 클럭이나 임계경로 설계와 관련된 공면(共面) 배선 구조에서의 신호선의 시그널 인테그러티를 검증하는 기법에 대한 새로운 방법을 통하여, GSG (ground–signal–ground) 와 PSG (power–ground–signal) 구조에서 시그널 인테그러티를 검증한다. 이를 통하여 클럭 배선에서 흔히 사용하는 GSG 배선구조는 PSG보다 더 많은 면적이 소요될 수 있다는 것을 보인다.

Abstract
This paper analyses and compares the signal integrity variations of two coplanar structures for on-chip provision of clock. It is believed that the on-chip area overhead caused by the Ground–Signal–Ground structure can be mitigated by a coplanar Power–Signal–Ground structure.

Keywords: Coplanar Waveguide Structure

I. Introduction
As the technology is towards its way to miniaturization, the interconnect lines play pivotal role in circuit performances[1]. In compact 3-dimensional ICs and packages, signals have to frequently travel through multi layers. However, sometimes it is not possible to ensure uninterrupted provision of ground (return path) to the signals close enough to ensure optimum performance. In digital domain, advantages of coplanar waveguide structures (CPW shown in Fig. 1(a)) over micro–strip, as a transmission medium used for on-chip global lines (such as clock, control lines and data busses) distribution are well known[2]. One of the advantages is the availability of the shortest return path for the signal on the same metal layer as of the signal but at the cost of area over head, i.e. less number of interconnects on that particular layer.

Our endeavor here is to look into the possibility of exploiting coplanar structure for provision of clock, yet minimizing the area overhead by using the structure shown in Fig. 1(b). In this paper we investigate and compare the performance of the coplanar transmission line structures as two different cases (Fig. 1(a) and (b) will be referred to as case 1 and case 2 respectively).

![Overall Self Capacitance](image-url)
II. Performance Evaluation for CPW lines

Topology presented in case 1 is very simple in terms of circuit model parameter extraction. However, parameters for case 2 (which can be represented as shown in Fig 2) are not straightforward to be extracted due to the power line. The problem arisen is, to find a way to obtain correct line parameters for case 2. In order to circumvent the problem, we came up with two different structures, as depicted in Fig. 3 (a) and (b) which are electrically equivalent to case 2 for separate extraction of capacitance and inductance respectively.

![Fig. 1. Coplanar Transmission Line Structure](image)

(a) Case 1: Ground-Signal-ground (gsg)
(b) Case 2: Power-Signal-Ground (psg)

![Fig. 2. Circuit Model for case 2 shown in Fig. 1(b).](image)

In this work, the analysis and comparison is based on the typical dimensional values of CPW structure and useful data as summarized in Table 1 [4]-[10]. Further, SiO$_2$ is selected as substrate with a dielectric constant of 3.9 and the line resistivity of Cu is taken to be 2.94 $\mu\Omega$-cm$^{[3]}$.

Typical figure of merits for comparison would be the 50% delay and overshoot/undershoot. Thus, assuming an on-chip clock frequency of 1GHz with a rise time of 10% of the clock period$^{[11]}$, the performance is investigated.

First, width of the signal line is varied from 1 $\mu$m–2 $\mu$m, keeping $w_s=s=1$ $\mu$m. As can be seen in Fig. 4 that there is not much of a difference in 50% delay time in both case 1(gsg) and case 2 (psg) for same width (about 10% for $w_s=1$ $\mu$m, and about 3% for $w_s=2$ $\mu$m). Slow rise time is due to the fact that generally the line resistance is in the range of 130 – 260 $\Omega$/cm$^{[6]}$ (in our case it is 147 $\Omega$ for $w_s=1$ $\mu$m and 73.75$\Omega$ for $w_s=2$ $\mu$m) so the RC delay is more. Case 2 structure (psg) can be noticed to be more inductive than case 1 (gsg).

![Fig. 3. Equivalent structures for case 2 (a) Structure for capacitance extraction (b) Structure for inductance extraction](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Interconnect Type</th>
<th>Width ($w$ $\mu$m)</th>
<th>Space ($s$ $\mu$m)</th>
<th>Length (L cm)</th>
<th>$Z_0$ ($\Omega$)</th>
<th>A/R ($t_{metal}/w$)</th>
<th>$R_S$ ($\Omega$)</th>
<th>$C_L$ (pF)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>On Chip</td>
<td></td>
<td>1–2 $^{[6]}$</td>
<td>$w$ $^{[6]}$</td>
<td>0.2–1.4$^{[6]}$</td>
<td>30–60$^{[6]}$</td>
<td>1 $^{[4]}$</td>
<td>&gt;0.5 $Z_0$ $^{[10]}$</td>
<td>1–2$^{[8]}$</td>
<td>[4][6][8][10]</td>
</tr>
<tr>
<td>Off Chip</td>
<td></td>
<td>10–100 $^{[7]}$</td>
<td>1.4$w$ – 2$w$ $^{[4]}$</td>
<td>40–70$^{[6]}$</td>
<td>25–100$^{[7]}$</td>
<td>0.2 – 0.6 $^{[4]}$</td>
<td>&gt;0.5 $Z_0$ $^{[10]}$</td>
<td>1–2$^{[8]}$</td>
<td>[4][7][8][10]</td>
</tr>
</tbody>
</table>
Next keeping $w_g = w_s = t_{metal} = 1 \mu m$, we varied the spacing(s) between the conductors from $1 \mu m - 2 \mu m$. It is clear from Fig. 5 that the difference in the simulated output of the two cases, is not much in terms of 50% delay, and overshoot/undershoot. Variation in the on-chip interconnect length is depicted in Fig. 6. For these simulations, we kept $w_g = w_s = s = t = 2 \mu m$. As mentioned in [5], As long as line resistance ($R_l$) ≤ $2Z_0$, the line has a fast rising response and acts as an LC circuit. As noticed in Fig. 6, $L = 5 \text{mm}$ gives an overshoot and undershoot of about 14%. Whereas for line $L = 10 \text{mm}$ it is about 7%. It is worth mentioning that this LC-type behavior can somewhat be controlled by dimensional optimization, basically reducing the capacitance. Here again, the comparison of the output waveform suggests case 2 to be an alternative of case 1 since there is no appreciable difference between the figure of merits.

Finally, load variation for a line with $w_g = w_s = s = t = 2 \mu m$ and length $L = 5 \text{mm}$ is shown in Fig. 7. For a load of 2pF, the output response in both the cases is delayed as theoretically expected, but here also, the difference in output for the two cases is not much which solidifies the previous deduction of case 2 being an alternative to case 1.
III. Conclusion

Two different CPW structures shown in Fig. 1 are analyzed and compared for provision of on-chip clock. A technique for per unit length parameter (PUL) extraction is developed for case 2, since it is not straightforward to extract them in 2D solver. Based on the simulation result, it is found that case 2 structure (Power-Signal-Ground) is more inductive than case 1 (Ground-Signal-Ground). An important finding is that with the same variation in different parameters in case 2 as in case 1, the difference in output of the two is within reasonable limits.

Having established the fact that the performance of the two structures do not differ much, the area overhead mitigated by case 2 structure is a lucrative advantage which makes the Power-Signal-Ground structure an alternative to the Ground-Signal-Ground structure.

References


