CAD Models and Verification of Integrated Circuit Interconnects

Yungseon Eo
Integrated Electronics Laboratory
Department of Electronic Eng.
Hanyang University

Phone: (0345) 400-5295
E-mail: eo@vlsi.hanyang.ac.kr

Abstracts

Interconnect models and their limitations are presented. The scattered materials pertinent to interconnects are investigated and then organized into some interesting topics, CAD model, parameters, and their experimental verification. Particularly signal delay, dispersion, reflection, crosstalk, and simultaneous switching noise, i.e., ground bouncing are the most important design issues for high performance circuit designs. Thus, their CAD models as well as model parameters are discussed. Particularly, since model verification becomes essential parts of modern integrated circuit design, some techniques are introduced. Further, in this paper, it is stressed that high speed circuits are not conventional low-frequency circuits but partly become microwave circuits. Currently, not only high frequency characterization based on the experimental analysis as well as more accurate CAD models are highly required, but also new design rules for circuit design must be developed. Thereby signal integrity can be guaranteed at the early stage of circuit design.

I. Introduction

Interconnects. They were simple signal path, however, they are now complex microwave circuits. As the chip size becomes larger and its performance becomes higher, interconnects become one of the most important design issues for both on-chip and off-chip [1]-[3]. Recently, since the most high performance VLSI circuits are switching in the sub-nano second, unlike
the conventional circuit design as in low frequency circuits, circuit designers without a doubt are plunged into the microwave world. Thus their accurate knowledge of interconnects in the microwave range is inevitable to design high performance VLSI circuits [4]–[6].

Interconnects can be divided into several sub-topics from the interesting view points or from other aspects. Nevertheless, they can be generically partitioned into some fundamental sub-groups. As an example, it can be divided into on-chip, off-chip, and between the two such as MCM (multi-chip module). Of course, their major impacts on the circuit designs or operations may somewhat differ from each other. However, its fundamental approaches to solve the problems or to design the circuit parameters are pretty much similar. Therefore, here the topics are subgrouped on the basis of the analytical points of view without distinguishing their physical formations. As long as we are interested in electrical problems of interconnects such as signal delay, reflection crosstalk, ground bouncing, and so forth, usually followings may be thought of as subsections,

1. simple CAD model and their parameters  
2. signal delay and dispersion model  
3. circuit models of multiple line interconnects (crosstalk)  
4. package interconnects  
5. experimental verification

Thus, the paper is organized as follows. First, the simple CAD models and parameters are introduced. Next the signal delay and dispersions are presented. Then multiple line models and analysis are discussed, followed by package problems. Finally, the experimental techniques are presented.

II. Simple CAD Model and Interconnect Parameters

From the microwave engineer’s point of view a interconnect, i. e. signal path is a kind of wave guide. Hence its exact analysis requires the solution of Maxwell’s equations with boundary conditions. However, in general its wave propagation mode is not simple TEM mode but it is TE mode which results in very complicated eigenvalue equations. Since it is too complicated to be analyzed even for very simple structures, many of the solution processes are approximated by quasi-TEM mode [7]–[9]. Then it can be mathematically much more simpler than before. That is, from the
microwave circuit points of view it can be mathematically modeled as Telegrapher Equations as in (1)

$$\frac{d^2 V(x)}{dx^2} = \gamma^2 V(x)$$ (1)

Once (1) is solved, it can be said that virtually everything can be disclosed. The above equation implies the knowledge of intrinsic characteristics of the given system. That is, characteristic impedance, Zo and propagation constant, \( \gamma \). The expression (1) will be extended to a matrix form for the multiple transmission lines. The first solution step for such matrix equation of multiple lines is to obtain the eigenvalues and eigenmatrix. However, unfortunately, they can not be readily yielded even for single line. Thus, here, for the simplicity's shake, we will consider only one transmission line. In the quasi-TEM mode, the characteristic impedance and propagation constant of the single line are presented as

$$Z_o = \sqrt{\frac{\frac{R + j\omega L}{G}}{\frac{G}{j\omega C}}}$$ (3)

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$$ (4)

Thus now again in order to calculate characteristic impedance and propagation constant, it is necessary to get transmission line parameters such as R, L, C, and G. In many packaging design, transmission line can be approximated as more simpler lossless mode. That is, in this case, if one can know L and C it is possible to predict signal transients. Whereas in the on-chip, resistance and capacitance have the significant effects on the circuit performances. Therefore in that case, simply R and C are the most important parameters. Among these parameters, conductor resistance can be readily extracted from both analytical manners or from experimental data. Therefore, only thing to be obtained is to get inductance and capacitance. From the analytical point of view, to calculate capacitance is much easier than the other, i.e. inductance. For lossless approximation as in off-chip interconnects, once the capacitance is known the inductance can be simply yielded by

$$LC = \mu_o \varepsilon_o$$ (5)
Thus it is apparent that capacitance is the most fundamental parameter for the simplest model as described. This is the reason why capacitance is prime interest in the first approximation model of interconnects.

There are numerous methods to yield capacitance model. They are Green function approach, empirical model, conformal mapping method, and usage of field-solver-based CAD tools, etc. The simple model can give the physical insights for the system but its accuracy is pretty limited. On contrast, CAD tool-based simulation gives good results with the sacrifice of design cost and time. As an example, Green function is to find electrostatic potential of the system as in

$$\phi(r) = \int_{D} G(r, r') \rho(r') dr'$$  \hspace{1cm} (6)$$

where $r$ is a observation point and $r'$ is a source point. The Green function can be interpreted as the impulse response. Once the integral equation is solved, the charge can be calculated, followed by the capacitance. Besides these, there are numerous methods to analyze the interconnect parameters. Interesting readers can refer to the literatures [8]-[16].

III. Signal Delay and Dispersion

Signal delay is the most important design parameter in the digital circuits. Particularly, as chip size becomes larger and the operation speed of circuits grows much faster, clock skew, glitches, and signal degradation, etc become more stringent. Thus, its accurate analysis at the beginning of the circuit design stage is essential. The signal delay on the interconnect is the very complicated phenomena which are entangled with many individual noise sources and circuit components. In many digital circuits, the first approximation of signal delay can be modeled as simple RC model. If the assumption is acceptable it is presented as [17]

$$t_{90\%} = (1.02 + 2.3(R_T C_T + R_T + C_T))RC \hspace{1cm} (7)$$

$$t_{50\%} = (0.377 + 0.693(R_T C_T + R_T + C_T))RC \hspace{1cm} (8)$$

However, such assumption is not always possible. In many high
performance circuits, critical path analysis plays a pivotal role to guarantee the circuit design success. The large portion of signal delay results from signal propagation delay due to phase delay and signal dispersion [6]. Fundamental reasons of signal dispersion are due to frequency-variant transmission line parameters such as skin effect of conductor and dielectric loss of substrate material. The skin effect loss of conductor can significantly reduce the propagation energy. However, it is only for wide and thick transmission lines as in package or global routing path such as clock or long data-bus lines within the chip. Whereas dielectric constant variations with frequency cause another signal loss. Particularly the silicon substrate signal loss cannot be neglected for modern VLSI circuits any more. Guckel and Hasegawa suggested that in the silicon substrate the signal propagate as pretty strange mode, what is called slow wave mode. It is due to dielectric polarization on the silicon substrate. Hasegawa modeled the effective dielectric constant as [18]

$$
\varepsilon_{\text{eff}} = \varepsilon_0 \varepsilon_s \left( \frac{d}{d_1} \right)
$$

(9)

where $d$ is the total dielectric thickness and $d_1$ is the oxide thickness. Since $d_1 \ll d$, the $\varepsilon_{\text{eff}}$ becomes very large. Thus, under this slow wave mode, signal propagates much more slowly than it was predicted in quasi-TEM mode. In facts, to understand their effects exactly make numerical simulation essential because conventional circuit simulation tools such as HSPICE or similar tools can not support these phenomena. As a bottom line, currently, the precise signal delay analysis for critical path necessarily requires the accurate model parameters of the given systems as well as complicated numerical simulation.

IV. Crosstalk and Multiline Interconnects

With the signal delay described in previous section, crosstalk is another issue that circuit designer must meet. Crosstalk is the signal coupling between the lines. As minimum feature size become smaller, its significance becomes more apparent. For example, in the 0.5um process, the worst case signal coupling restricts the circuit design flexibilities even though process can permits its capabilities. They naturally increase the design cost and limit
the circuit density. Particularly in the current VLSI and next generation ULSI circuits, the design limitation due to interconnect crosstalk can make its process success virtually useless.

Many one have tried to solve the problems in the frequency domain. The first reason to characterize them at frequency domain is because interconnect parameters and its system function are more easily formulated at the frequency domain [19]. However, since the circuit designer needs the time domain responses any way. The frequency domain function requires inverse transform into the time domain. On the other hand, the CAD tools require the simple but accurate closed-form-model for simulation. That is, from the layout information, they want to directly extract noise levels. Thus many literatures show the simple crosstalk models. However, they have fundamental limitation for both accuracy and its generality. Recently many researchers try to solve these problems by introducing the waveform relaxation approach. Most active researches have been done in the AWE (Asymptote Waveform Evaluation) [20][21]. The AWE is to use Pade Approximation, thereby without the time consuming Fourier transform the time domain signal transients can be estimated. The approach generally presents the interconnect transfer function as rational function,

\[
H(s) \approx \frac{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + 1}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + 1} \tag{10}
\]

and then \( H(s) \) can be modified into the product of factors by using Pade Approximation,

\[
H(s) \approx \frac{Q(s)}{P(s)} \tag{11}
\]

Then with Heaviside Theorem and residue calculation, inverse Laplace transform can yield the time domain response

\[
h(t) \approx \delta(t) + \sum_{i=0}^{n} q_i e^{-\mu_i t} \tag{12}
\]

Ultimately, with the modified nodal analysis, the transients simulation in the given circuits can be yielded with convolution integral. Since convolution integral is another time consuming procedure, Lin et al introduced the
recursive convolution integral [21]. However, many literatures report that this approach causes stability problems due to non-convergence. Although many algorithms to improve stability are suggested, it seems to be inherent problems of this approach because it neglects the higher order terms during the moment matching. Furthermore, it inherently fail to treat the frequency variant transmission lines without resorting to curve fitting. Thus this approach may have limitations in the dispersive media.

V. Simultaneous Switching Noise and Package Interconnects

The most serious problem relevant to IC packaging is simultaneous switching noises [23]–[25]. It is called as another name of delta-I noise. That is, Most ICs necessarily require bonding wires between outside signal path to die pads. It is relatively long signal path. As the logic blocks within a chip switch, they let the current flow from the die to the ground or pull up the charges from voltage source to the die. Since such a switching is dynamic behavior, it instantaneously induces the voltage across the lead frame inductance. This voltage changes the die ground line potential or power line. Thereby these cause to fluctuate the reference potential and then become a source of malfunctions of the circuits. It can be simply modeled as [23]

\[ V_{ssn} = V_k + \frac{V_{kt}}{2nV_{DD}L_{pK}} \left[ 1 - \sqrt{1 + \frac{4nV_{DD}L_{pK}}{t_r}} \right] \] (13)

As it is shown in the expression, simultaneous switching noise (ground bounce) is strongly related to the rising time, length of leadframe, and output load capacitance etc. However, they cannot be simply avoided by circuit designer. There are many techniques to reduce such noises by using BGA (Ball Grid Array) packaging, impedance matching, decoupling capacitance, and optimal placements of ground and power.

The SSN is increased with high-density and high-speed of the VLSI chip as well as the physical configuration. The MCM described in the previous section may increase these noises while promising technology for high speed operation. The typical packaging solutions to reduce the SSN noise are BGA (ball grid array), and QPSK. Such techniques are fundamentally to reduce the inductance shortening the signal path length. It should be noted that just reduction of signal path can not completely solve the problems. Thus
new design schemes should be developed. Further, decoupling capacitance can reduce the power fluctuation. The role of decoupling capacitance is to supply the charge within a short time during the switching. In practical situation, such noises are entangled with signal reflection and crosstalk. Thus, to guarantee overall signal integrity and successful design, the accurate CAD models considering other signal noises make it possible to improve high performance circuit design. The interconnect problems in MCM are basically similar to other interconnect problems.

VI. Experimental Verification

Currently most of the CAD models related with interconnects are not experimentally verified. Moreover, it is very difficult to experimentally prove them because they are microwave circuits. In many cases the verification of transmission line parameters resorts to numerical field solver or indirectly commercially available circuit simulation. Within a limited bound, it may be acceptable. However the modern fine line interconnects which are very lossy and may be predominated by fringing effects show discrepancy with the exact values [6][26].

Experimental verifications need microwave characterization techniques using scattering parameters as well as parasitic de-embedding at the frequency domain or TDR and TDT techniques at the time domain [26][27]. Otherwise the verification in microwave is virtually impossible. Unfortunately, in some special test patterns, the experimental data of existing CAD models and parameters reflect pretty significant digress from simulation. Thus, without exact verification of model parameters, the accuracy of circuit simulation itself cannot be expected. This is very important fact since existing process-based or simulation-based circuit design rules must be modified in more detailed level. In addition, it should be noted that, to improve the accuracy of the CAD models the experimental verification will become essential parts of high performance circuit design and new verification techniques must be developed.

VII. Conclusion

The critical performance bottleneck of the next generation of the state of the art VLSI circuits may be due to interconnect. VLSI interconnect and
package interconnects play a pivotal role in high performance VLSI circuits.

In this paper, existing interconnect CAD models and their parameters are introduced. Since each model has its own fundamental limitations, circuit designers must caution for selecting or using suitable CAD models. Furthermore, without accurate physical understanding the interconnects, high performance VLSI circuit designer may cope with very serious design failures. Moreover, most of current interconnect models have not be experimentally verified. Although limited, the experimental data show that the currently used models have far amount of deviation from theoretical values. Thus the blind use of models without the accurate verification of them is very risky. Currently process-based design rules must be reconsidered with the electrical testing. Then in more detail, the design rules must be developed for each semiconductor fabrication processes. Finally, although they are not discussed in this paper, thermal heating and electromigration may be significant problems that the circuit designer may challenge to improve sooner or later.

REFERENCES


