Abstract—This paper analyses and compares two Coplanar Structures to be employed as shielded structures for on-chip critical interconnect lines such as clock. It is believed that at lower bit rates, on-chip area overhead caused by the Ground-Signal-Ground structure can be mitigated by a coplanar Power-Signal-Ground structure, if the performance of the two is not much different. However at higher bit rates, in addition to area saving, the later structure is shown to be better performance wise.

Keywords-component: Coplanar Waveguide, Transmission lines, Signal Integrity

I. INTRODUCTION

As the technology is towards its way to miniaturization, the interconnect lines play pivotal role in circuit performances [1]. In compact 3-dimensional ICs and packages, signals have to frequently travel through multi layers. Due to noise effects, critical lines should be shielded. However sometimes it is not possible to ensure uninterrupted provision of ground (return path) to the signals close enough to ensure optimum performance. In digital domain, advantages of coplanar waveguide structures (CPW shown in Fig. 1(a)) over microstrip, as a transmission medium used for on-chip global lines (such as clock, control lines and data buses) distribution are well known [2]. One of the advantages is the availability of the shortest return path for the signal on the same metal layer as of the signal but at the cost of area over head, i.e. less number of interconnects on that particular layer.

Our endeavor here is to look into the possibility of exploiting coplanar structure for provision of critical interconnect lines (such as clock), yet minimizing the area overhead by using the structure shown in Fig. 1(b). In this paper we investigate and compare the performance of the coplanar transmission line structures as two different cases (Fig. 1(a) and (b) will be referred to as case 1 and case 2, respectively).

The organization of the paper is as follows. In section II, issues related to line parameters extraction for the two structures are addressed, which is of utmost importance for simulating the response of a transmission line. Subsequently in section III, detailed parametric analysis and comparison of both structures based upon practical data is given. In addition comparison of eye openings and jitter for both structures is also presented giving an insight to the signal quality. Section IV concludes the paper.
then just by rearranging first row of $C$

If we consider power line modeled as signal 1 in sgs structure, unchanged for case 2. Thus extraction, the next goal is to simulate the CPW structures of case 1 and 2, and compare the results. Our intent here is not to characterize the interconnect lines, which has already been extensively done [3][4][6]-[10]. Therefore the analysis and comparison carried out in this work is based on the typical dimensional values of CPW structure and useful data as summarized in Table 1.

In our simulations, we assume copper conductor (for its lower resistivity and less electromigration effects) and SiO$_2$ as substrate with a dielectric constant of 3.9 [11]. As per ITRS 2007, resistivity of Cu is taken to be 2.94 $\mu$Ω-cm [12]. Although on-chip clock frequency was predicted to increase by a factor of 2 per generation in ITRS 2000, going over 15GHz by 2010 (ITRS 2003), but due to some serious impediments, most significant of which is limitation from maximum allowable power dissipation [12][13], practically attainable on-chip frequency is around 1GHz - 4GHz [13]. For this work on-chip clock frequency of 1GHz is considered with a rise time of 10% of the clock period [14] (although for eye opening analysis higher data rates are also considered). Typical figure of merits in comparison are 50 % delay, overshoot/undershoot and of course the eye opening of the two cases. We take $w_s = w_a = s$. In order to maintain an aspect ratio of 1, $t_{metal} = w_i$ is considered. The driver impedance for this analysis is taken to be 20 $\Omega$ [15], and a load of 0.1pF is used.

First of all width of the signal line is varied, keeping $w_a = s = 1$µm. Fig. 4 shows the responses for the two cases, for two different values of the signal line width range. As can be seen in Fig. 4 that there is not much of a difference in 50% delay time in both case 1(GSG) and case 2 (PSG) for same width (about 25% for $w_i = 1$µm, and about 10% for $w_i = 2$µm).

Rising time gets faster for the lines with lesser resistance as can be seen for line with $w_i = 2$ µm (73.75 $\Omega$) as compared to one with $w_i = 1$ µm (147 $\Omega$). Case 2 (PSG) can be noticed to be slightly more inductive than case 1(GSG). This inductive effect, however, becomes more pronounced as the bit rate increases. To exemplify, Fig. 5 shows the response for the two cases with varying line width at 10 Gbps. This fact remain valid for all subsequent on-chip parametric analysis and clearly calls for an eye opening comparison for the two cases which is presented later in this section.

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**III. SIGNAL INTEGRITY EVALUATION**

Having developed a scheme for the PUL line parameter extraction, the next goal is to simulate the CPW structures of case 1 and 2, and compare the results. Our intent here is not to characterize the interconnect lines, which has already been extensively done [3][4][6]-[10]. Therefore the analysis and
Next keeping $w_g = w_s = t_{metal} = 1 \mu m$, we vary the distance $s$, between the conductors. As can be seen in Fig. 6, the differences in the simulated output of the two cases are not significant in terms of 50% delay, and overshoot/undershoot at lower bit rate. The scenario is the same at higher bit rate as shown in Fig. 5 (i.e. inductive effect is more in case2).

Variation in the on-chip interconnect length is depicted in Fig. 7. For these simulations, we kept $w_g = w_s = s = t_{metal} = 1 \mu m$. As mentioned in [6], as long as line resistance ($R_L$) $\leq 2Z_0$, the line has a fast rising response and acts as an LC circuit. As the line length thus resistance ($R_L$) is increased and tends to exceed twice the characteristic impedance of the line ($2Z_0$), the rise time is slowed down. This phenomenon can be seen in Fig. 7, i.e. the shortest line being more inductive and resistance being the lowest has the fastest rising time.

It is worth mentioning that this LC- type behavior can somewhat be controlled by dimensional optimization, basically reducing the capacitance. Here again, the comparison of the output waveform suggests case 2 to be an alternative of case1 at a bit rate of 1Gbps since there is no appreciable difference between the figure of merits.

Load variation for a line with $w_g = w_s = s = t_{metal} = 1 \mu m$ and length 5mm is shown in Fig. 8. For a load of 1pF, the output response in both the cases is delayed as theoretically expected, but here also, the difference in output for the two cases is not significant which solidifies the previous deduction of case 2 being an alternative to case 1 at lower bit rate.

Fig. 9 compares the eye opening and jitter for the two cases at different data rates. Eye opening is plotted for a line with $w_g = w_s = s = t_{metal} = 1 \mu m$ and length of 5mm. It is an established fact that with increase in data rates the eye opening decreases [16]. The phenomenon can be viewed in Fig. 9 for case1 and case2. At lower data rates ($\leq 5$Gbps), the performances of the two cases are almost equally good. However, at higher data rates, in addition to area over head mitigation, case2 promises to be of an advantage in terms of eye opening and jitter also. Reference [17] suggests that for effective high speed signaling

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**TABLE I. TYPICAL VALUES OF INTERCONNECT DATA AND DIMENSIONS**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Width ($w \ \mu m$)</th>
<th>Space ($s \ \mu m$)</th>
<th>Length ($l \ \text{cm}$)</th>
<th>Ch. Impedance $Z_0 \ \Omega$</th>
<th>Aspect Ratio ($t_{metal}/w$)</th>
<th>Source Impedance $\Omega$</th>
<th>Reference</th>
</tr>
</thead>
</table>
beyond 10 Gbps, resistive termination is required. Optimal resistive termination can be employed to enhance the eye opening of the two cases improving bandwidth at the cost of lower signal amplitude, area and power dissipation [16].

![Figure 8. Varying load for L=5mm: Response of case1 and case 2](image1)

Figure 8. Varying load for L=5mm: Response of case1 and case 2

![Figure 9. Eye opening and Jitter: Response of case1 and case 2](image2)

Figure 9. Eye opening and Jitter: Response of case1 and case 2

### IV. CONCLUSION

Two different CPW structures shown in Fig. 1 are analyzed and compared as shielded systems of interconnects used for critical on-chip signals such as clock. For an accurate analysis, a technique for per unit length parameter (PUL) extraction is developed for case 2, since it is not straightforward to extract them in 2D solver. Based on the simulation result, it is found that case 2 structure (Power-Signal-Ground) is more inductive than case 1 (Ground-Signal-Ground). An important finding is that with the same variation in different parameters in case 2 as in case 1, the output of the two is within reasonable limits at lower bit rates (≤ 5Gbps). At higher bit rates, however inductive effect in case2 is more pronounced and a judicial selection of geometry of Power-Signal-Ground promises better performance for on chip provision of clock (by virtue of wider eye opening and less jitter). The stated advantage along with the area overhead mitigated by case 2 structure is a lucrative incentive which makes the Power-Signal-Ground structure an alternative to the Ground-Signal-Ground structure. It implies that at bit rates up to 5Gbps, arbitrary selection of case1 or case2 works (if we keep area overhead aside for a moment) due to their comparable performance. But at higher bit rates, it is a different story and the selection calls for a much careful analysis of the two structures as presented.

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