Experimental Via Characterization for the Signal Integrity Verification of Discontinuous Interconnect Line

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Abstract—Interconnect lines with inter-layer vias are experimentally characterized by using high-frequency S-parameter measurements. Test patterns are designed and fabricated using a package process and measured using Vector Network Analyzer (VNA) up to 25 GHz. Then, by modeling a via as a circuit, its model parameters are determined. It is shown that the circuit model has excellent agreement with the measured S-parameters. The circuit performance of the lines with inter-layer vias is evaluated by using the developed circuit model. Thereby, it is shown that via may have a substantially deteriorative effect on the signal integrity of high-speed integrated circuits.

Keywords—circuit model; eye-diagram; S-parameter; via

I. INTRODUCTION

Over the last four decades, the circuit switching speed and level of integration of integrated electronic systems have dramatically improved [1]. Today's high-performance integrated circuits operate over several GHz of operating frequencies and a several tens (10s) of Gbps data rate. Recent System In a Package (SIP) or three-dimensional (3D) integration technologies make even more tremendous progress in system performance and the level of the integration [2]-[6]. The higher level of integration inevitably requires the more inputs/outputs (I/Os) and induces more complicated routing congestion. In such systems, an array area I/O arrangement with a tight physical pitch is very common, which necessitates many vias for physical layout.

In next generation high-speed communication systems such as Ethernet or Synchronous Optical NETwork (SONET), high-speed chips with data rates of more than 100 Gbps are required [7]-[9]. Additionally, high-speed data-processing modules such as Serialization and De-serialization (SerDes) require a several 10s of Gbps data rate in SIP or Printed Circuit Board (PCB) level (i.e., outside of chips). All of these imply that interconnect latency tends to dominate the system performance rather than the gates [10]. Therefore, the circuit reliability and data bandwidth are increasingly limited by the signal integrity exacerbation due to interconnect lines [10], [11].

Since vias change the impedance of a signal path, they may cause substantial signal deterioration in high-speed system due to reflection and additional phase variation. While the via effects have to be taken into account in the early phase of circuit design, the characterization of the via is not straightforward. One of the reasons for this is that vias are not uniform transmission line structures [13]. There have been many techniques to characterize and model vias [14]-[23], however, most of them are based on numerical calculation [14]-[16], commercial field solvers [17], [18], or simple closed form models [19], [20].

In this work, vias are characterized and modeled with high-frequency S-parameters. Further, it is shown that vias may induce substantial signal integrity deterioration in high-speed integrated system.

II. EXPERIMENTAL CHARACTERIZATION

A. Motivation for High-Frequency Via Characterization

In order to investigate the extent of the effect of vias on the signal integrity, the S-parameters of the line including a pair of vias are compared with straight lines as shown in Fig. 1. Although the total length of the line including the vias is 2.1 mm, its S21 characteristic is comparable to the 10 mm long straight line. Furthermore, existing techniques have fundamental limitations. Not only do very high-frequency measurements cost too much, but also the co-planar structure measurements are very error-prone due to the parasitics. In addition, since a via is considered to be a two-port network, special test pattern and measurement techniques are required. In a package process, 10 % process variations in both the dielectric thickness and metal pitch are typical. Thus, it is too hard to accurately calculate the via characteristics by using field solver.

B. Experimental Characterization of Vias.

Since a via is too tiny in its size to be accurately characterized in high-frequencies by using SMA connectors that may induce large parasitic effects during measurements, a
Figure 1. S-parameter measurement data.

Figure 2. Test patterns.

Figure 3. Conceptual description of electromagnetic field distribution for the circuit model of the test structure.

Figure 4. Circuit models of the vias.

coplanar contact technique is preferred to SMA connectors. The planar circuit probing for 2-port network measurements requires a pair of contact pads (GSG, Ground-Signal-Ground) on the same plane. Otherwise, two port measurements may not be possible. Thus, two vias should be considered a pair for the via characterizations. That is, one is an upper layer to lower layer via and the other is a lower layer to upper layer via.

Furthermore, although the access lines between the contact pad and the via are necessary, they have to be de-embedded for an accurate characterization. Test patterns for planar interconnect line characterization are designed and fabricated on the same substrate as the via patterns. The test patterns and its cross-sectional dimensions are described in Fig. 2

A VNA for the test pattern measurements is calibrated by a Short, Open, Load, and Thru (SOLT) calibration method up to probe tips. Then, S-parameters for the test patterns including access lines are measured from 50 MHz to 25 GHz by using microwave probe tips (Cascade Microtech GSG probe tips). Note, although access lines are inevitable for planar circuit measurements, the effects have to be de-embedded for an accurate characterization. Thus, a 0.5 mm long line is designed on the same test module for the purpose of parasitic effect de-embedding.

III. EXPERIMENTAL PARAMETER DETERMINATION

Considering the electromagnetic field distribution of a signal line through two vias as schematically described in Fig. 3, a via may be represented by one of the two possible circuit models: a T-type and a Pi-type model as shown in Fig. 4.

Test pattern measurement system can be represented by cascaded ABCD or T-network. In order to de-embed the parasitic access line effects, the measured S-parameter data of the test structure are represented by using ABCD matrices

\[
[ABCD]_{\text{total}} = [ABCD]_{\text{line}} [ABCD]_{\text{DUT}} [ABCD]_{\text{line}}^{-1}. \quad (1)
\]

Therefore, the de-embedded S-parameters for DUT (device under test) can be readily determined as

\[
[ABCD]_{\text{DUT}} = [ABCD]_{\text{line}}^{-1} [ABCD]_{\text{total}} [ABCD]_{\text{line}}^{-1}. \quad (2)
\]

In the T-type model of Fig. 4(a), the measured S-parameter data can be equated by using the ABCD network parameters as follows

\[
[ABCD]_{\text{DUT}}^{T} = \begin{bmatrix}
1 + Z_{j} & Z_{j} & Z_{j} & Z_{j} \\
Z_{j} & Z_{j} & Z_{j} & Z_{j} \\
1 & 1 & 1 & 1 \\
Z_{j} & Z_{j} & Z_{j} & Z_{j}
\end{bmatrix}, \quad (3)
\]

where the measurement reference impedance \(Z_{0} = 50[\Omega]\). Thus, the circuit model parameters for the T-type network can be determined as follows.

\[
\text{Im}(1/Z_{j})/\omega = \text{Im}(C)/2\pi f = C_{\text{via}}^{T}, \quad (4)
\]

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\[
\text{Im}(Z_v) / \omega = \text{Im}(\frac{(D-1)/C}{2\pi f}) = \frac{1}{L_{\text{via}}}.
\]

Similarly, since the ABCD parameters for the Pi-type circuit model are

\[
[ABCD]_{\text{DUT}} = \begin{bmatrix}
\frac{1}{Y_i} & \frac{1}{Y_i} \\
\frac{1}{Y_i} & \frac{1}{Y_i} \\
\end{bmatrix},
\]

then the circuit model parameters can be determined by

\[
\text{Im}(Y_i) / \omega = \text{Im}(\frac{(D-1)/B}{2\pi f}) = \frac{C^\pi_{\text{via}}}{L_{\text{via}}},
\]

\[
\text{Im}(1/Y_i) / \omega = \text{Im}(B)/2\pi f = \frac{L^\pi_{\text{via}}}{L_{\text{via}}}.
\]

The total inductances and total capacitances for each circuit model are defined, respectively, as

\[
L_{\text{total}} = 2L^T_{\text{via}} + L^\pi_{\text{via}},
\]

\[
C_{\text{total}} = C^T_{\text{via}} + C^\pi_{\text{via}}.
\]

The total inductances and total capacitances of the test structure are compared in Fig. 5. Note, regardless of the circuit model type (T-type or Pi-type) of the test structure, the circuit model parameters show excellent agreement up to 5 GHz. On the contrary, as the frequency increases, large discrepancy becomes evident. This is considered to be due to the different lumped circuit models. Therefore, the circuit model parameter values are averaged in 100 MHz to 5 GHz range. The total inductance and total capacitance are 0.26 nH and 0.26 pF, respectively. Thus, the T-type and Pi-type models can be represented by the extracted circuit model parameters. However as shown in Fig. 6, it is considered that the T-type circuit model for the via test structure is better than the Pi-type circuit model.

**IV. SIGNAL INTEGRITY VERIFICATION**

In order to investigate via effects, the three types of practical interconnect systems are considered as shown in Fig. 7. Although the straight length between both ends of all of the structures is 2 cm long, the S-parameter data for the three types of line structures (i.e., a line with no via, a line with 2 vias, and a line with 4 vias) are determined by using the proposed circuit model and compared in Fig. 8. It becomes evident that vias have a significant effect in high-frequencies.

An eye-diagram is a very helpful metric for intuitively and quickly assessing the performance quality of digital signals. That is, the performance of circuits can be easily estimated with jitter and eye-opening using the eye-diagram. Eye-diagrams are, in general, determined by overlapping the continual output responses for numerous Pseudo-Random Bit Sequence (PRBS) input signals. In order to verify the signal integrity of interconnect lines with inter-layer vias, the test circuits as shown in Fig. 7 are employed. Then the circuit performance is evaluated in terms of eye-opening and jitter. With design variables such as data rate and the number of vias, eye-diagrams using 50,000 bits of PRBS are determined.

In order to clearly show the signal deterioration due to vias, eye-diagrams for 5 Gbps and 20 Gbps are compared in Fig. 9. Obviously, the signal integrity is much more seriously exacerbated in 20 Gbps data rate rather than in 5 Gbps. As expected, vias have a significant effect on signal deterioration. Possibly, with longer line lengths and more vias, signal integrity deterioration may be substantial even in low data rate circuits.
Figure 9. Eye-diagrams: Eye-opening is significantly deteriorated with vias in high-data rate links.

V. CONCLUSION

A via has a deteriorative effect on the signal integrity of high-speed integrated circuits and packages. In this work, interconnect lines with inter-layer vias were experimentally characterized up to 25 GHz. Then, modeling the via with the T-network, the circuit model parameters were directly determined by using the measured S-parameters. The circuit performance of the lines with vias can be efficiently evaluated by using the developed circuit model in terms of eye-opening with various circuit design variables. It was shown that the vias have a significant effect on signal deterioration. Particularly, the higher bit rate, the more significant the signal integrity degradation due to vias becomes.

REFERENCES