Efficient Eye-Diagram Determination Technique of Non-Linearly-Switching Coupled-Data Links Under Power and Ground Fluctuation Noises

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Abstract

A novel eye-diagram determination technique for coupled data links driven with the non-linear drivers is proposed. The non-linear characteristics of the driver are pre-characterized for a given circuit topology using SPICE step responses. Input test vectors that constitute eye-boundaries are found. The eye-diagram is determined with the test vectors. It is shown that the proposed technique is much more efficient than that of the PRBS-based generic technique in the order of two, whereas its accuracy is similar to that of the PRBS-based SPICE simulation (less than 5% error in both eye-height and jitter).

Keywords-component: eye-diagram; inter-symbol-interference; simultaneous switching noise.

Introduction

As the switching frequency and the level of integration of integrated circuits drastically increase, data links between the circuit blocks become one of the crucial system design issues [1]. The signal integrity degradation of the data links is mainly due to i) signal loss in interconnect lines, ii) reflections due to discontinuity, iii) electromagnetic coupling, and iv) power/ground supply noise during the circuit switching. Conventional piecemeal timing analysis and electromagnetic coupling analysis of data links are not sufficient enough to fully reflect the aforementioned physical phenomena.

In order to evaluate the holistic circuit performance, the inter-symbol-interference (ISI) is usually investigated. The ISI can be readily evaluated with the eye-height, eye-width, and jitter using the eye-opening at the destination node of a channel [2], [3]. Generically, the eye-diagram can be determined with SPICE simulation, applying numerous pseudo random bit sequence (PRBS) to the input of the circuit. Even if the technique is accurate, however, it requires huge amount of computation time and hardware resources. For example, in order to determine the accurate eye-diagram, PRBS input data more than \(2^{17} \cdots 2^{180} \) are at least required. In practice, SPICE simulation using such large number of input data may not be acceptable in multi-coupled data links because of the large computation time and hardware resources. In order to overcome such an impractical problem, numerous techniques that are computationally efficient have been developed [2]-[6].

The peak distortion analysis (PDA) algorithm (or similar techniques) [4] that approximates the input driver circuit as a voltage source with a linear resistor is a representative technique. However, it has a fundamental limitation to be employed for non-linear circuits. As a TX (input driver) is inherently non-linear and asymmetrically switching, the PDA analysis is too inaccurate to be acceptable in practical circuits. Although the double-edge response (DER) approach [5], [6] improves the PDA problems a bit, the accuracy is still not sufficient enough to be employed for the evaluation of the practical circuits that are electromagnetically coupled and contaminated with various noises during circuit switching.

In this work, an accurate and efficient eye-diagram determination technique for the signal integrity verification of electromagnetically coupled data links with non-linear drivers that include simultaneous-switching-noise (SSN) is proposed. The inherent non-linear properties of drivers are pre-characterized with step responses using SPICE simulation. Next, possible input test vectors (i.e., bit streams) that constitute eye boundaries are found. Then, the eye-diagram for the channel is determined using SPICE simulation with the input test vectors. Finally, for a practical test circuit that is comprised of non-linear drivers with SSN, the accuracy and efficiency of the proposed technique are verified.

Test Vectors and ISI Determination

Signal transients in coupled lines are strongly dependent upon input switching patterns. Since a signal for each line may have one of the three switching states, (i.e., rising state, quiet state, and falling state), the switching pattern for the coupled lines is one of the 9 possible patterns. Given a circuit topology, these switching patterns should be pre-characterized with step responses using SPICE simulation that reflect the almost all of the non-linear characteristics for the given system. With the pre-characterized step responses, the input test vectors that constitute the eye-diagram boundaries are determined as follows. First, the number of the significant input bit stream is determined. A step response is settled down after a time elapses. Thus, since a present signal is affected by the tail signals of the previous signals until all the previous signals are settled down, the length of the input bit patterns \((m)\) is defined as

\[
m \equiv \left\lfloor \frac{t_{\text{settle}}}{T_b} \right\rfloor, \tag{1}
\]

where \(t_{\text{settle}}\) is the settling time and \(T_b\) is an one bit duration time. Thus, the significant input bit stream vector of the \(i\)-th line can be represented by

\[
[B_i] = \begin{bmatrix} b_{i0} & \cdots & b_{i1} & \cdots & b_{i0} \end{bmatrix}, \tag{2}
\]

where the \(b_{i0}\) indicates the present bit of the \(i\)-th line and the \(b_{ij}\) indicates the \(j\)-th previous bit of the \(i\)-th line. Note that an eye-diagram is composed of eight eye-boundaries, which is indicated with the subscript \(z \in \{1, 2, \cdots, 8\} \). Thus, in two coupled lines, the significant input bit stream can be represented with a matrix form,
\[
\begin{bmatrix}
B_i \\
B_2
\end{bmatrix} =
\begin{bmatrix}
\begin{array}{cccc}
1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0
\end{array}
&
\begin{array}{cccc}
2 & 2 & 2 & 2 \\
2 & 0 & 2 & 0
\end{array}
\end{bmatrix}.
\tag{3}
\]

Secondly, in the interested line, since the present bit state may be either of 1 (logic high) or 0 (logic low) state, the state of the present bits of the two coupled lines are one of the 4 possible states. The response signals of the first two previous bit pairs, \(\{b_{10}, b_{11}\}\) and \(\{b_{20}, b_{21}\}\), can be readily evaluated using the pre-characterized step responses. Since the worst response or the best response may be eye-boundaries, they are set as input test vectors. Similarly, using the greedy algorithm for all the previous bit stream, their switching patterns are iteratively evaluated with the \(T_c\)-delayed step responses using the same decision criteria. Then the final input test vectors are used for SPICE input test vectors for the eye-diagram determination.

**Verification**

In order to verify the accuracy and efficiency of the proposed technique, a test circuit as described in Fig. 1 is evaluated. The eye-diagrams for the test circuit using both PRBS-based SPICE simulation and the proposed technique are determined (see Fig. 2) and summarized in Table 1. The proposed technique shows an excellent agreement with the PRBS-based SPICE simulation using \(2^{17}\)-PRBS input bits as shown in Fig. 2. The eye-opening data (height and jitter) using the proposed technique show excellent agreement with those of PRBS-based SPICE simulation (less than 5% error), whereas the computation time is much faster in the order of two. Note that other conventional techniques show large discrepancies although the computation time is reasonable.

**Conclusion**

In this paper, a new efficient eye-diagram determination technique for the signal integrity verification of non-linearly switching coupled data links is proposed. The non-linear characteristics of drivers are pre-characterized with the switching-dependent step responses using SPICE simulation. Using the step responses, the input test vectors for the worst eye-diagram are determined with a newly developed algorithm. Finally, the worst eye-diagram can be accurately and quickly determined using SPICE simulation with the input test vectors.

**Table I**

<table>
<thead>
<tr>
<th>Tech.</th>
<th>Eye-Determination Tech.</th>
<th>SPICE (217-bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Opening</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Height [mv]</td>
<td>752.0 (+4.7%)</td>
<td>1006.9 (+40.2%)</td>
</tr>
<tr>
<td>Jitter [ps]</td>
<td>35.7 (-4.5%)</td>
<td>19.8 (-47.1%)</td>
</tr>
<tr>
<td>Time [s]</td>
<td>64.2</td>
<td>53.9</td>
</tr>
</tbody>
</table>

The efficiency and accuracy of the proposed technique was verified with a practical test circuit with non-linear drivers under SSN noises. The simulation results show excellent agreement with those of PRBS-based SPICE simulation, whereas the computation time is much faster in the order of two. Therefore, the proposed technique can be efficiently exploited for the high-speed data link design.

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**References**


